Finally in step S35, INDEX_8 is stored back to the packet index buffer 40 by the microprocessor 60, thereby completing a microprocessor-to-port transfer procedure.

In summary, the present invention provides a new switching hub architecture and the index-shared network packet transfer method, which may be suitably employed on a switching hub to carry out various packet transfer procedures in a more efficient manner. Since the proposed switching hub architecture and index-shared packet transfer method thereof is characterized in that the embedded packet-switching control unit and microprocessor are both capable of retrieving a packet index from the same packet index buffer that indicates an unoccupied packet buffer area in the packet buffer memory, the packet flow control mechanism can be executed by the packet transfer queue circuitry such that packet transfer efficiency can be improved.

The above descriptions are only illustrative of the preferred embodiments of the present invention, and are not intended to limit the scope of the essential technique of the present invention. The scope of the invention is broadly defined by the claims appended hereto. If any physical forms or methods implemented by the others are identical or equivalent to those defined in the claims below, they are considered to be within the scope of the claims.